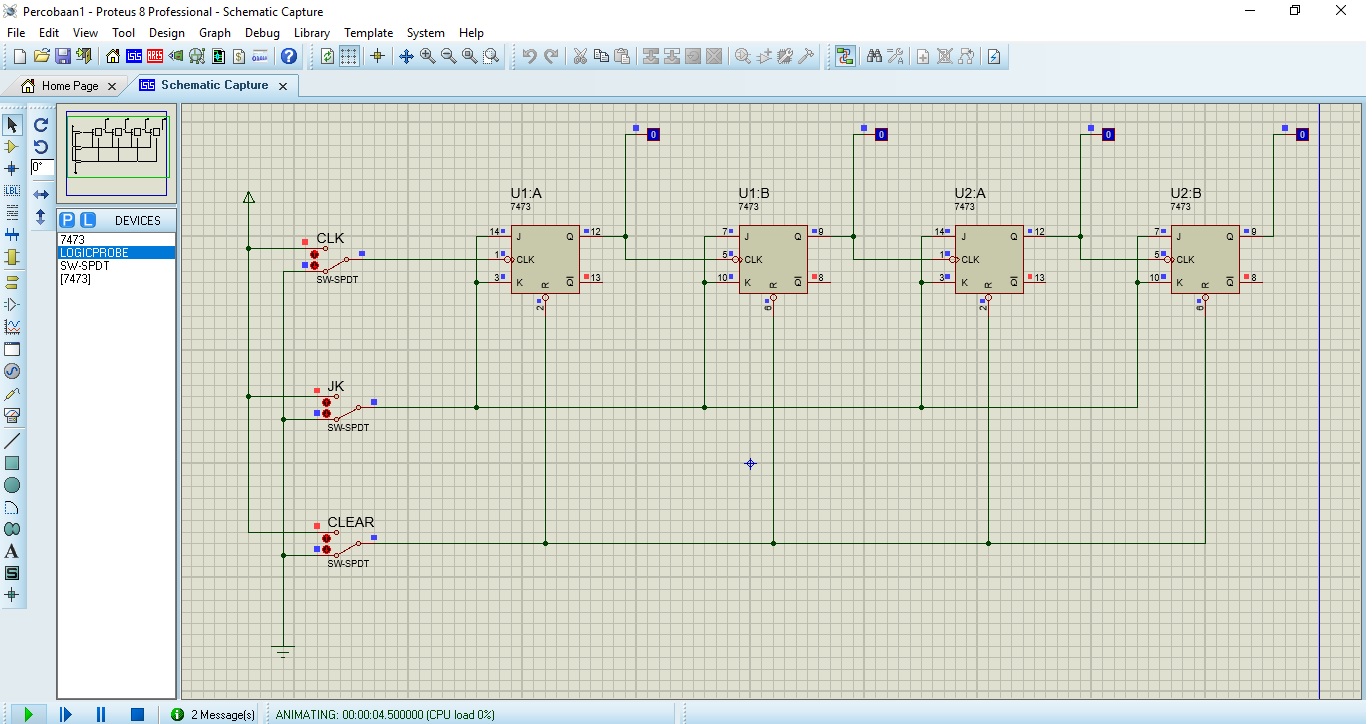
**Modul 8**

Nama : Andrias Sigid W.R

NIM : L200144010

Percobaan 1

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | INPUT | | | OUTPUT | | | |
| CEAR | JK | CLK | A | B | C | D |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 4 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 5 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 6 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 7 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 8 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 9 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 10 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 11 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 12 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 13 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 14 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 15 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 16 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 17 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 18 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 19 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 20 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

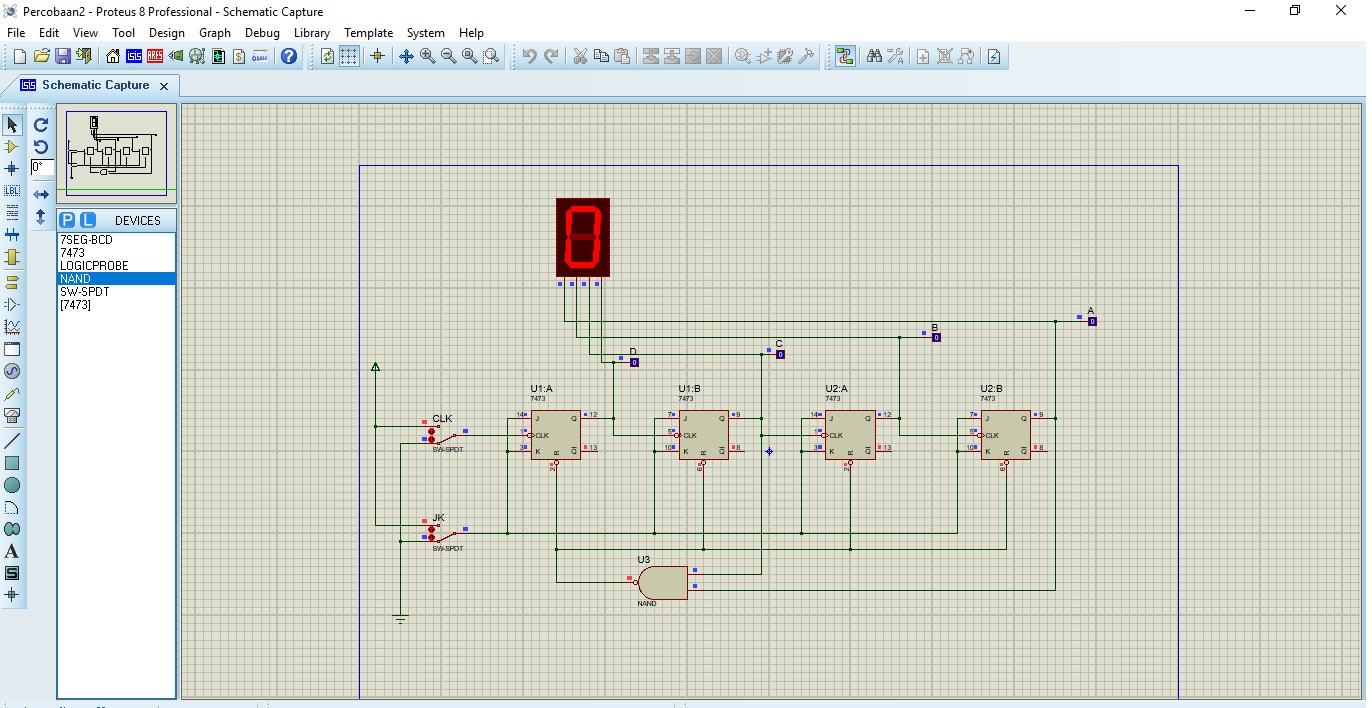
1. a. Fungsi CLK : menghidupkan atau switch on/off pada clock

b. Switch JK : menghidupkan / switch on/off pada JK FlipFlop

c. Swictch CLEAR : Switch on/off untuk mereset

1. Kesimpulan : terjadi perubahan pada output ketika switch CLK diubah dari k enol yang bermula pada percobaan ke 3 dari posisi switch CLK 1

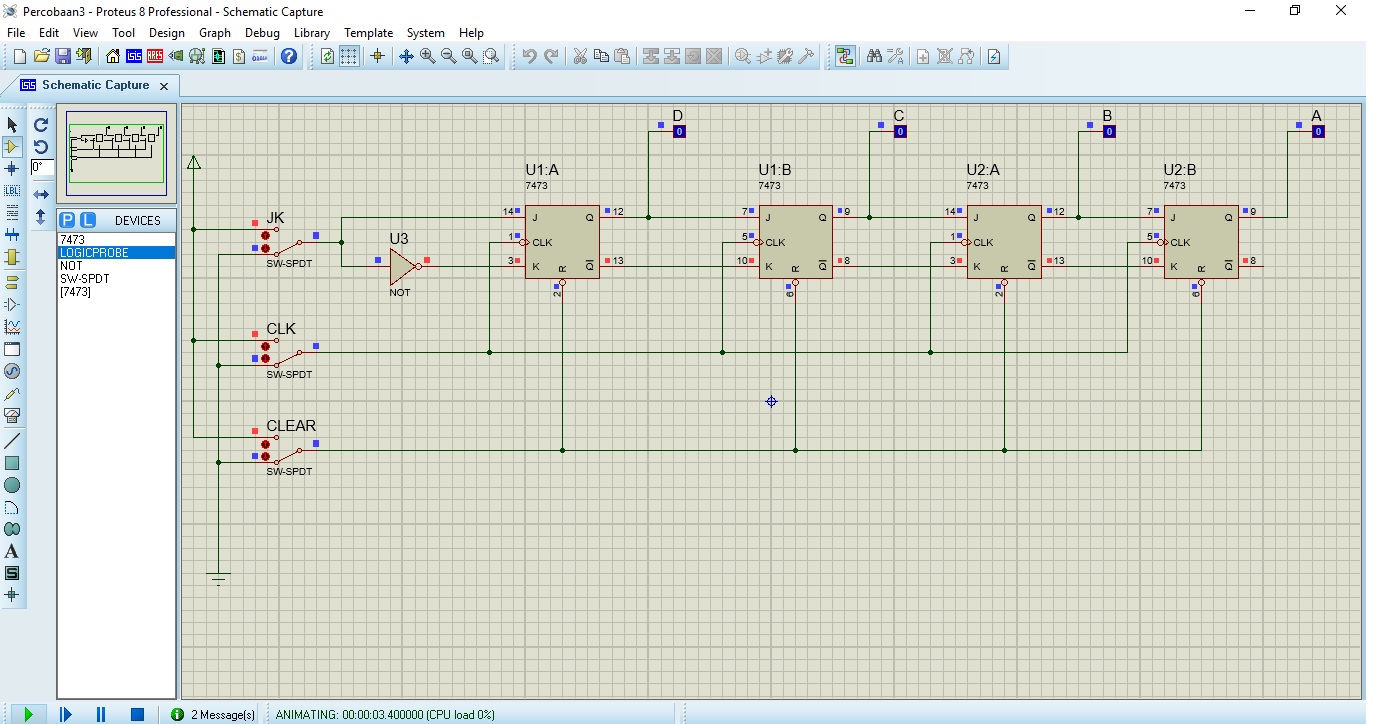
Percobaan 2



|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | INPUT | | OUTPUT | | | |
| CEAR | JK | A | B | C | D |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 1 | 1 | 0 | 0 | 0 | 0 |
| 3 | 1 | 0 | 0 | 0 | 0 | 1 |
| 4 | 1 | 1 | 0 | 0 | 0 | 1 |
| 5 | 1 | 0 | 0 | 0 | 1 | 0 |
| 6 | 1 | 1 | 0 | 0 | 1 | 0 |
| 7 | 1 | 0 | 0 | 0 | 1 | 1 |
| 8 | 1 | 1 | 0 | 0 | 1 | 1 |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 |
| 10 | 1 | 1 | 0 | 1 | 0 | 0 |
| 11 | 1 | 0 | 0 | 1 | 0 | 1 |
| 12 | 1 | 1 | 0 | 1 | 0 | 1 |
| 13 | 1 | 0 | 0 | 1 | 1 | 0 |
| 14 | 1 | 1 | 0 | 1 | 1 | 0 |
| 15 | 1 | 0 | 0 | 1 | 1 | 1 |
| 16 | 1 | 1 | 0 | 1 | 1 | 1 |
| 17 | 1 | 0 | 1 | 0 | 0 | 0 |
| 18 | 1 | 1 | 1 | 0 | 0 | 0 |
| 19 | 1 | 0 | 1 | 0 | 0 | 1 |
| 20 | 1 | 1 | 1 | 0 | 0 | 1 |
| 21 | 0 | 0 | 1 | 0 | 0 | 1 |
| 22 | 0 | 1 | 1 | 0 | 0 | 1 |
| 23 | 1 | 0 | 0 | 0 | 0 | 0 |
| 24 | 1 | 1 | 0 | 0 | 0 | 0 |

Kesimpulan : Saat switch JK dan CLK kondisi 1 dari 0 tidak terjadi perubahan, terjadi perubahan jika JK dan CLK kondisi 1 dan 1 lalu diubah lagi menjadi 1 dan 0 hingga berulang 9x pada 7SEG lalu di reset ke 0.

Percobaan 3.



|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | CEAR | JK | CLK | A | B | C | D |
| 1 | 0 | x |  |  |  |  |  |
| 2 | 1 | 1 |  |  |  |  |  |
| 3 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 4 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 5 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 6 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 7 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 8 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 9 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 10 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 11 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 12 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 14 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 16 |  |  |  |  |  |  |  |

Kesimpulan : terjadi perubahan output pada saat switch clock diubah ke nol dari yang awalnya 1